BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The invention may best be understood by referring to the following description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

[0007] Figure 1 illustrates an exemplary system 100 comprising processors 102 and 104 for translating atomic constructs, according to embodiments of the present invention.

[0008] Figure 2 illustrates a data flow diagram for generation of a number of executable program units that include instances of an atomic operation according to one embodiment of the invention.

[0009] Figure 3 is a flow chart for translating an atomic operation according to one embodiment of the invention.

[0010] Figure 4 is a diagram illustrating a program unit being translated into a second program unit according to one embodiment of the invention.

[0011] Figure 5 is a flow chart for performing the translated program unit 405 according to one embodiment of the invention.

[0012] Figure 6A is a diagram illustrating threads encountering the WRAPPER_FXN of the program unit 405 of Figure 4 according to one embodiment of the invention.

[0013] Figure 6B is a diagram illustrating the thread 603 performing an exemplary operation of the program unit 405 according to one embodiment of the invention.

[0014] Figure 6C is a diagram illustrating the thread 603 determining atomicity of the memory update operation according to one embodiment of the invention.

[0015] Figure 6D is a diagram illustrating the thread 605 performing the loop of the program unit 409 according to one embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0016] In the following description, numerous specific details are set forth to provide a thorough understanding of the invention. However, it is understood that the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the invention.

[0017] Figure 1 illustrates an exemplary system 100 comprising processors 102 and 104 for translating atomic constructs, according to embodiments of the present invention. Although described in the context of system 100, the present invention may be implemented in any suitable computer system comprising any suitable one or more integrated circuits.

[0018] As illustrated in Figure 1, computer system 100 comprises processor 102 and processor 104. Computer system 100 also includes processor bus 110, and chipset 120. Processors 102 and 104 and chipset 120 are coupled to processor bus 110. Processors 102 and 104 may each comprise any suitable processor architecture and for one embodiment comprise an Intel® Architecture used, for example, in the Pentium® family of processors available from Intel® Corporation of Santa Clara, California. Computer system 100 for other embodiments may comprise one, three, or more processors any of which may execute a set of instructions that are in accordance with embodiments of the present invention.

[0019] Chipset 120 for one embodiment comprises memory controller hub (MCH) 130, input/output (I/O) controller hub (ICH) 140, and firmware hub (FWH) 170. MCH 130, ICH 140, and FWH 170 may each comprise any suitable circuitry and for one